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8-Bit Integrated Optical SNS ADC

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Abstract

Recently, a new technique has been described for extending the resolution of an integrated optical multi-interferometer analog-to-digital converter (ADC). These types of ADCs can directly digitize the signals from an antenna and play an important role in eliminating the need for intermediate frequency and baseband processing. With resolution greater than 12 bits, these types of architectures are useful for a variety of applications. The new technique is based on the incorporation of a symmetrical number system (SNS) encoding to provide high resolution (greater than 1-bit per interferometer) while also reducing the complexity of the optical hardware. In this paper we present recent developments on an 8-bit design using this approach.

1 Background

The most efficient (sampling) ADCs demonstrated to date use integrated electro-optical guided-wave technology (in lithium niobate, gallium arsenide, or indium phosphide). Symmetrical folding of the input signal is realized with Mach-Zehnder Interferometric (MZI) waveguide modulators arranged in a parallel configuration [1–3]. These modulators use the linear Pockels effect and provide a convenient method for coupling a wideband electrical signal into an optical processing system through the modulator electrodes.

Recently, a technique that extends the resolution of an integrated optical multi-interferometer analog-to-digital converter was described [4–5]. The optical output waveform for each interferometer is symmetrically folded at twice a proper modulus. A small comparator ladder mid-level quantizes each interferometer's detected output to encode the analog signal in a symmetrical number system (SNS) format. By incorporating the SNS encoding, resolution greater than 1-bit per interferometer can be provided.

The SNS is composed of a number of pairwise relatively prime (PRP) moduli m_i. The integers within each SNS modulus are representative of a symmetrically folded waveform with the period of the waveform equal to twice the PRP modulus. For m given, the integer values within twice the individual modulus are given by:

$$x_m = [0, 1, \cdots, m-1, m-1, \cdots, 1, 0] \quad (1)$$

The SNS folding waveform is symmetrical about the midpoint and is compatible with other folding waveforms. Due to the presence of ambiguities, the integers within Eq. (1) do not form a complete system of length $2m$ by themselves. It is well known however, that the inclusion of additional redundant moduli can effectively detect and correct errors within a residue number system (RNS) representation of a number. The SNS formulation is based on a similar concept which allows the ambiguities to occur. The ambiguities that arise within the SNS are resolved by using various arrangements of the SNS moduli. By considering the derived moduli arrangements, the SNS is rendered a complete system having a one-to-one correspondence with the residue number system. For N equal to the number of PRP moduli, the dynamic range M of the system is [4]

$$M = \prod_{i=1}^{N} m_i \,. \quad (2)$$

The SNS can serve as a source for resolution enhancement in an ADC by decomposing the analog amplitude analyzing function into a number of parallel sub-operations (moduli) that are of smaller computational complexity. Each sub-operation for a different modulus requires only a precision in accordance with that modulus. A much higher resolution is achieved after the results of these low precision sub-operations are recombined. That is, the resolution of each interferometer can be increased beyond 1 bit

per interferometer. A schematic diagram of the SNS ADC architecture is shown in Fig. 1. The input signal is folded in parallel with each folding period equal to twice a particular modulus. The folded waveform at the output of each folding circuit is mid-level quantized with a small comparator ladder to encode the input signal in the SNS format. An encoder then converts the SNS representation to a more familiar digital output such as a binary representation. With the SNS encoding any combination of folding periods and comparator arrangements can be analyzed exactly.

The optical output power from a single guided-wave interferometer is symmetrical and periodic and can thus be used to implement each folding circuit (modulus) in the SNS ADC. The interferometer normalized output is a function of both the sampled analog voltage v and the modulus m_i as

$$I(v,m) = \cos^2\left(\frac{\pi v}{2m_i} + \frac{\pi}{2}\right) . \tag{3}$$

That is, the voltage dependent phase shift $\Delta\phi_i = \pi v/2m_i$. In terms of the electro-optical parameters

$$\Delta\phi_i = KL_i v \tag{4}$$

where L_i is the length of the electrode and K is a constant that depends on the index of refraction, the electro-optic coefficient, the interelectrode gap, the electrical-optical overlap parameter, and the optical wavelength. Thus, the electrode lengths vary as

$$L_i = \frac{\pi}{Km_i} \tag{5}$$

or inversely proportional to m_i. Note from (5) the requirements to double the electrode length between each interferometer is eliminated. Also, since the moduli are PRP and can be chosen to be similar in magnitude, the electrode lengths are also similar in size. The advantage here is that the interferometers (folding circuits) in the system can be identical devices. The small electrode length difference that is required for each modulus, can be instrumented by placing a small attenuator at the analog input.

The folding circuit for each modulus requires $m_i - 1$ comparators at the output of the detector. With the waveform given by (3), the normalized threshold values for the comparators within each modulus m_i are

$$T_{i,j} = \cos^2\left(\frac{\pi v_j}{2m_i} + \frac{\pi}{2}\right) \tag{6}$$

where

$$v_j \in \{1, 2, 3, \cdots, m_i - 1\} . \tag{7}$$

That is, the comparator thresholds are tailored to the interferometer output waveform. The size of the least significant bit (LSB) for the SNS ADC is

$$V_{\text{LSB}} = \frac{V_\pi}{m_{\min}} . \tag{8}$$

where $m_{\min}$ is the smallest modulus.

Figure 2 shows an interferometer output waveform which has a period of 10 volts. Also shown are four comparator thresholds. Using this waveform as the folding waveform for modulus 5, we obtain the SNS comparator output (thermometer code) which is cyclic in nature and shown in Table 1. Note the modulus can always be scaled to any particular folding period. For example, if the interferometer folding period is 4 volts, the comparator thresholds can be easily adjusted to implement a modulus 5. Table 2 gives several possible SNS ADC configurations. Systems with resolution on the order of 7 to 11-bits are shown. Detailed are the modulus corresponding to each interferometer, the dynamic range M, the total number of comparators required, and the maximum number of comparators loaded in parallel at a detector output (fan out).

2 Design Considerations

The SNS ADC employs integrated optical interferometers to preprocess the analog signal. Each interferometer folds the input signal at a particular PRP modulus m_i and a small comparator ladder is used after each detector to detect the various voltage levels and encode the input signal into the SNS format. The normalized interferometer output can be expressed as

$$I = \frac{1}{2} + \frac{1}{2}\cos\left[\Delta\phi(v) + \pi\right] . \tag{9}$$

The voltage dependent phase shift $\Delta\phi(v)$ for a push-pull electrode configuration can be expressed in terms of the electro-optic parameters as

$$\Delta\phi(v) = \frac{2\pi n_e^3 \Gamma L_i v}{G\lambda} , \tag{10}$$

where n_e is the effective index of the optical guide, r is the pertinent electro-optic coefficient, G is the interelectrode gap, Γ is the electrical-optical overlap parametr, and λ is the free-space optical wavelength. One important performance specification for an integrated optical interferometer is the amount of electrode voltage needed to transition the normalized output from a minimum ($\Delta\phi = 0$) to a maximum ($\Delta\phi = \pi$). This voltage V_π is

$$V_\pi = \frac{G\lambda}{2L_i n_e^3 r\Gamma} . \tag{11}$$

Another device constraint is the maximum voltage that may be applied to the electrodes. Applied voltage beyond the rated maximum (minimum) will spark across the electrode structure and damage the device. The specifications of V_π and $v_{\max}$ reveal the maximum number of folds available from the device. A complete fold is $2V_\pi$. The maximum number of folds F available from a device is therefore

$$F = \frac{2v_{\max}}{2V_\pi} . \tag{12}$$

The smallest modulus within the SNS system requires the largest number of folds to instrument the dynamic range M. Since a complete fold is $2V_\pi = 2m_i$, The largest number of folds required from an interferometer in a B-bit SNS ADC is

$$F_{\text{req}} = \frac{2^B - 1}{2m_{\min}} < \frac{v_{\max}}{V_\pi} , \tag{13}$$

where $m_{\min}$ is the smallest modulus in the SNS system.

3 Decimation of Errors

Within the SNS ADC, the folding waveforms and comparator levels together divide the input voltage into M regions of equal size. The points at which the folding waveforms cross the comparator thresholds all occur at the same input voltage. The SNS can present a problem at each of these specific voltage levels. The threshold levels need to be crossed simultaneously for several or all moduli. When some comparators, at a position to change, do change, while others do not, the recovered amplitude will have a large error. The probability of this occurrence depends upon the offset voltage match of the comparators, the tolerance of the voltage dividing resistors and the corresponding width of the input voltage region being affected. In other words, we can accept the fact that a small portion of the sampled voltage levels will fall in this critical range and give false amplitudes.

The other alternative is to discard the errors using a few additional comparators. On the least modulus, m_1, we use $2m_1$ comparators rather than $m_1 - 1$. Of these, $2m_1 - 2$ would be paired, one just below the proper comparator threshold level and the other just above. Of the other two, one would be just above the minimum modulation depth, and the other threshold just below the maximum detector output. Let us assume that a signal arrives and all comparators below a certain level are on. This is as it should be. For each incoming signal, if it turns on an *even* number of comparators, $0, 2, 4, \cdots, 2m_1$, the signal is rejected. If it turns on an *odd* number of comparators, it is accepted. In this manner we place a narrow band around each voltage level that corresponds to a switching point. For all other moduli, the comparator levels are adjusted so that they fall within these narrow bands. Any input signal within these narrow rejection bands can be easily discarded.

4 Performance Characteristics

The 8-bit SNS ADC uses a sampling frequency $f_s = 5$ MHz and contains three parallel channels. The three interferometers being used were built by the Naval Research Laboratory and are on loan from the National Security Agency. The maximum voltage that can be applied to these devices is $v_{\max} = \pm 30$ volts. The V_π is 2.1 volts (minimum modulus). The total number of folds available from each device is 14. Using (13), the minimum modulus is calculated as $m_{\min} = 9$. Since the channel moduli must be pairwise relatively prime the remaining two channels are $m_2 = 10$ and $m_3 = 11$. From (8), the size of the LSB is 233 mv. Including the few additional comparators for error decimation, the total number of comparators required is 37, with a maximum of 18 loaded in parallel.

The 8-bit 5 MHz SNS ADC is near completion. All digital boards are built and tested and are currently being integrated to the optical processor front end. A preliminary test was performed on the digital processor using LabView™ to emulate the three interferometer output waveforms. The transfer function is shown in Fig. 3. In this case the decimation width was 0% of the LSB (no decimation). Note the presence of the encoding errors. In Fig. 4, the decimation width is increased from 0% of the LSB to 10% of the LSB. Note the decrease in the number of errors present.

5 Conclusions

In this paper we demonstrate the performance of an 8-bit SNS ADC which employs three interferometers (three channels) and 22 comparators.

Acknowledgements

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Table 1: Modulus 5 Comparator States

Input Voltage	Number of Comparators "ON"
0 to 1	0
1 to 2	1
2 to 3	2
3 to 4	3
4 to 5	4
5 to 6	4
6 to 7	3
7 to 8	2
8 to 9	1
9 to 10	0

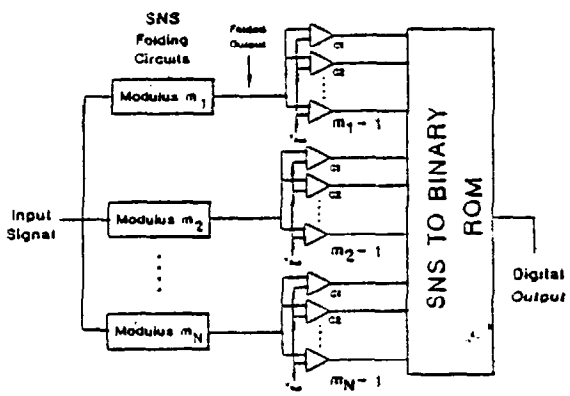

Figure 1: Optimum SNS ADC architecture.

Table 2: SNS ADC Parameters

Interferometer Moduli	M	Total Number of Comparators	Max Number Loaded in Parallel	Number of Bits (b)	$F_{req} < V_{max}/V_\pi$
11, 12	132	21	11	7	5.8
3, 4, 5, 7	420	15	6	8	42.5
3, 5, 7, 8	840	19	7	9	85.5
9, 10, 13	1170	29	12	10	57.1
13, 14, 15	2730	39	14	11	78.7

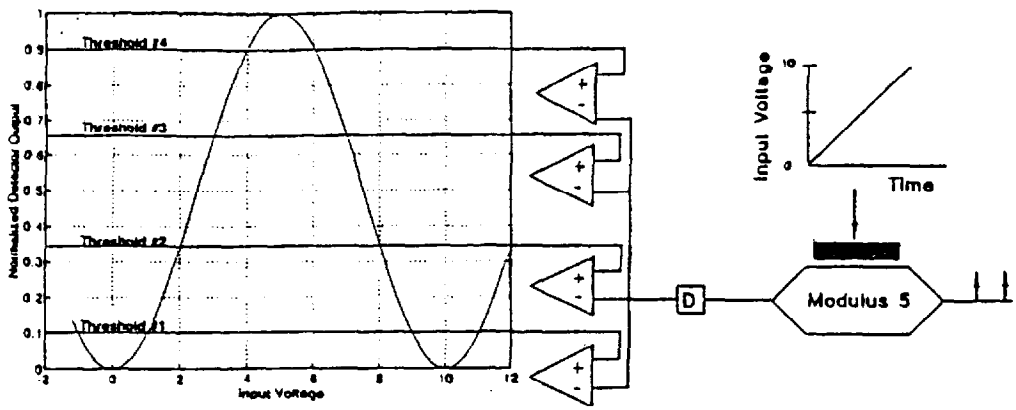

Figure 2: Modulus 5 channel.

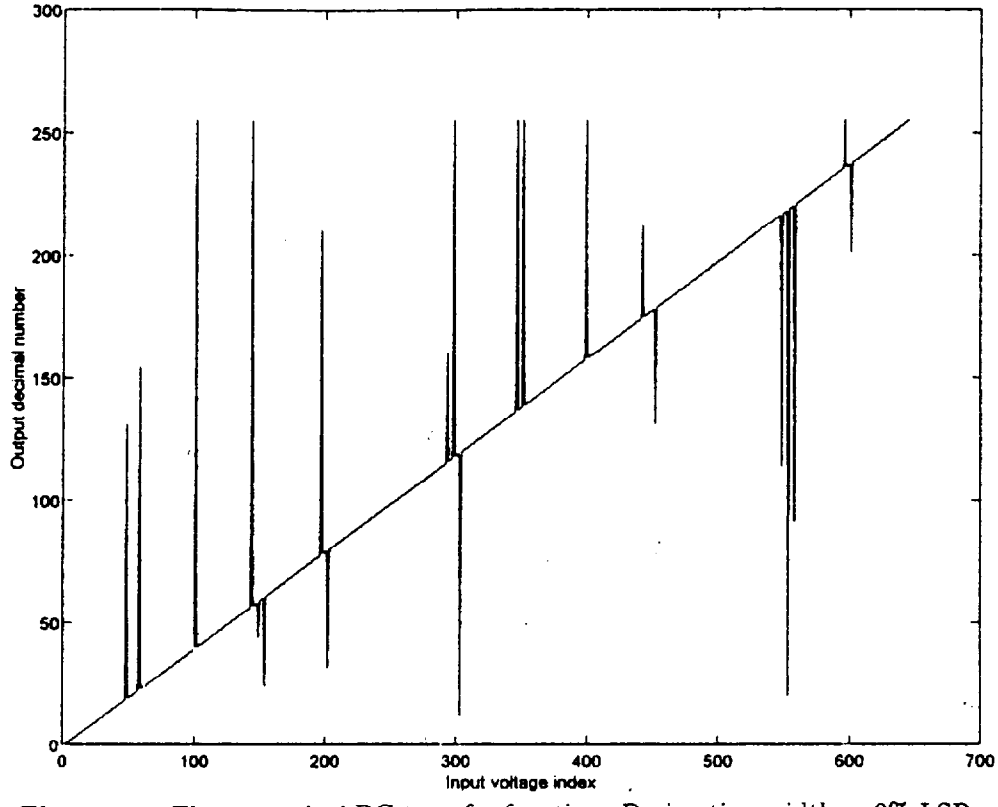

Figure 3: Electro-optic ADC transfer function: Decimation width = 0% LSB.

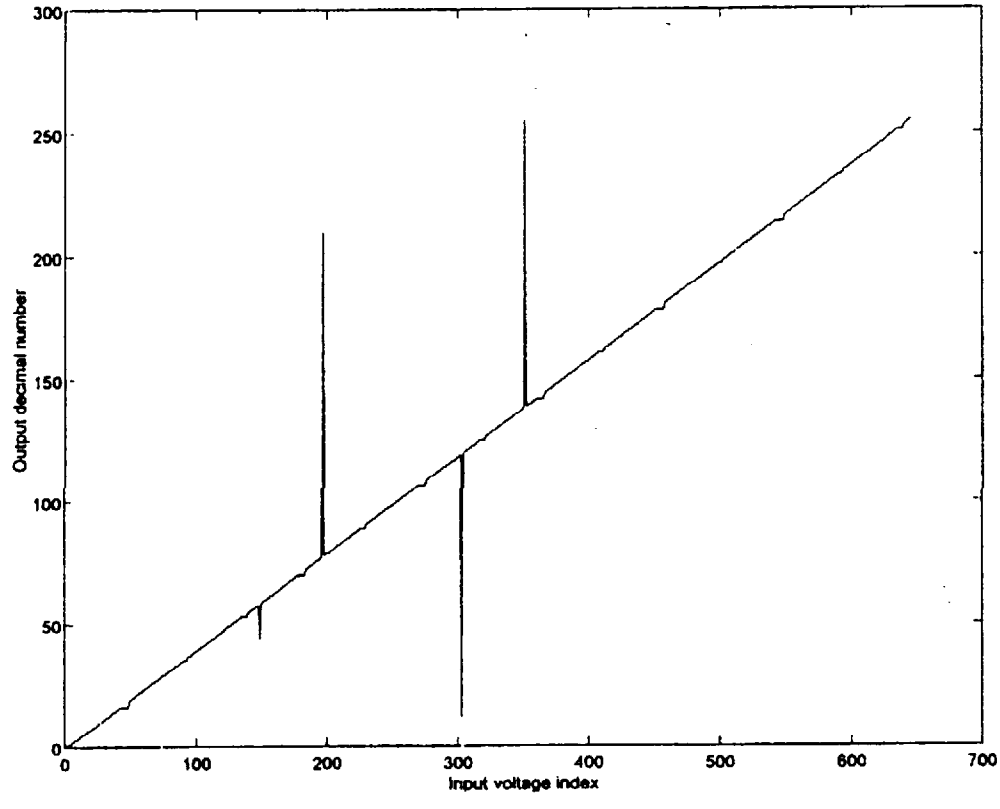

Figure 4: Electro-optic ADC transfer function: Decimation width = 10% LSB.